ABSTRACT

Disclosed is a semiconductor die having a plurality of dummy fillings positioned and sized to minimize defects during chemical mechanical polishing is disclosed. At least one of the dummy fillings is coupled to an underlying test structure. In a preferred embodiment, the semiconductor die also includes a plurality of conductive layers and a substrate. The underlying test structure includes a first layer portion formed from a first one of the plurality of conductive layer and a via coupling the first layer portion to the at least one dummy filling. In another aspect, the underlying test structure also has a via coupling the first layer portion to the substrate, and the underlying test structure comprises a plurality of layer portions and vias to form a multilevel test structure.

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